IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A digital true random number generator circuit, comprising: ~~a linear feedback shift register having an input and an output, a system clock having a system clock frequency value for driving said shift register, and a free-running oscillator operatively connected to said input of said shift register, said generator circuit further comprising at least one further free-running oscillator operatively connected to said input, said oscillators and said system clock having different oscillation frequency values, the greatest common divisor of which having the value one~~

a linear feedback shift register having an input and an output;

a plurality of free-running oscillators each operatively connected to a separate input of a single exclusive OR-circuit;

said exclusive OR-circuit having an output operatively connected to an input of a latching circuit;

said latching circuit having an output operatively connected to the input of said linear feedback shift register and configured to drive said linear feedback shift register; and

a system clock operatively connected to a clock input of said latching circuit and having a system clock frequency value configured to drive said linear feedback shift register,

wherein said free-running oscillators and said system clock have different oscillation frequency values, the greatest common divisor of the different oscillation frequency values having the value one.

Claim 2 (Original): A digital true random number generator circuit according to claim 1, wherein each free-running oscillator is designed as a ring oscillator having a plurality of cascade connected inverter circuits in a sequence and an output.

Claim 3 (Original): A digital true random number generator circuit according to claim 2, wherein each ring oscillator has an odd number of inverter circuits.

Claim 4 (Currently Amended): ~~A digital true random number generator circuit according to claim 2,~~ A digital true random number generator circuit, comprising:

a linear feedback shift register having an input and an output;

a system clock having a system clock frequency value for driving said linear feedback shift register; and

a plurality of free-running oscillators operatively connected to said input of said linear feedback shift register,

wherein said free-running oscillators and said system clock have different oscillation frequency values, the greatest common divisor of the different oscillation frequency values having the value one,

each free-running oscillator is designed as a ring oscillator having a plurality of cascade connected inverter circuits in a sequence and an output, and

~~wherein~~ each ring oscillator has an odd number of inverter circuits and the number of inverter circuits of each ring oscillator ~~differ~~ differs by two.

Claims 5-6 (Canceled).

Claim 7 (Currently Amended): A digital true random number generator circuit according to claim [[6]] 1, wherein said latching circuit is a D-type flip flop.

Claim 8 (Currently Amended): ~~A digital true random number generator circuit according to claim 1,~~ A digital true random number generator circuit, comprising:

a linear feedback shift register having an input and an output;

a system clock having a system clock frequency value for driving said linear feedback shift register; and

a plurality of free-running oscillators operatively connected to said input of said linear feedback shift register,

wherein said free-running oscillators and said system clock have different oscillation frequency values, the greatest common divisor of the different oscillation frequency values having the value one,

said linear feedback shift register has a plurality of n cascade connected delay stages, said stages being divided into a first sub-plurality of i stages having an output operatively connected as a first input to ~~a further~~ an exclusive OR-circuit[[;]], i and n being positive integers,

said output of said linear feedback shift register being operatively connected to an input of a NOR-circuit[[;]],

said NOR-circuit having an output which operatively connects to a second input of said ~~further~~ exclusive OR-circuit[[;]], and

said ~~further~~ exlusive OR-circuit having ~~a third input which forms~~ an output configured to drive and forming the input of said linear feedback shift register~~, for driving said register~~.

Claim 9 (Original): A digital true random number generator circuit according to claim 8, wherein i <= n.

Claim 10 (Currently Amended): An Application Specific Integrated Circuit (ASIC) comprising:

a digital true random number generator circuit, said generator circuit comprising, ~~a linear feedback shift register having an input and an output, a system clock having a system clock frequency value for driving said shift register, and a free-running oscillator operatively connected to said input of said shift register, said generator circuit further comprising at least one further free-running oscillator operatively connected to said input, said oscillators and said system clock having different oscillation frequency values, the greatest common divisor of which having the value one~~

a linear feedback shift register having an input and an output,

a plurality of free-running oscillators each operatively connected to a separate input of a single exclusive OR-circuit,

said exclusive OR-circuit having an output operatively connected to an input of a latching circuit,

said latching circuit having an output operatively connected to the input of said linear feedback shift register and configured to drive said linear feedback shift register, and

a system clock operatively connected to a clock input of said latching circuit and having a system clock frequency value configured to drive said linear feedback shift register,

wherein said free-running oscillators and said system clock have different oscillation frequency values, the greatest common divisor of the different oscillation frequency values having the value one.

Claim 11 (Currently Amended): An encryption device, comprising:

means for encrypting; and ~~provided with~~

a digital true random number generator circuit, said generator circuit comprising, ~~a linear feedback shift register having an input and an output, a system clock having a system clock frequency value for driving said shift register, and a free-running oscillator operatively connected to said input of said shift register, said generator circuit further comprising at least one further oscillator operatively connected to said input, said oscillators and said system clock having different oscillation frequency values, the greatest common divisor of which having the value one~~

a linear feedback shift register having an input and an output,

a plurality of free-running oscillators each operatively connected to a separate input of a single exclusive OR-circuit,

said exclusive OR-circuit having an output operatively connected to an input of a latching circuit,

said latching circuit having an output operatively connected to the input of said linear feedback shift register and configured to drive said linear feedback shift register, and

a system clock operatively connected to a clock input of said latching circuit and having a system clock frequency value configured to drive said linear feedback shift register,

wherein said free-running oscillators and said system clock have different oscillation frequency values, the greatest common divisor of the different oscillation frequency values having the value one.

Claim 12 (Currently Amended): A transactions terminal, comprising:

means for performing transactions; and ~~provided with~~

a digital true random number generator circuit, said generator circuit comprising, ~~a linear feedback shift register having an input and an output, a system clock having a system clock frequency value for driving said linear feedback shift register, and a free-running oscillator operatively connected to said input of said linear feedback shift register, said generator circuit further comprising at least one further free-running oscillator operatively connected to said input, said free-running oscillators and said system clock having different oscillation frequency values, the greatest common divisor of which having the value one~~

a linear feedback shift register having an input and an output,

a plurality of free-running oscillators each operatively connected to a separate input of a single exclusive OR-circuit,

said exclusive OR-circuit having an output operatively connected to an input of a latching circuit,

said latching circuit having an output operatively connected to the input of said linear feedback shift register and driving said linear feedback shift register, and

a system clock operatively connected to a clock input of said latching circuit and having a system clock frequency value configured to drive said linear feedback shift register,

wherein said free-running oscillators and said system clock have different oscillation frequency values, the greatest common divisor of which having the value one.